REMARKS

The examiner has rejected claims 1-12 under 35 U.S.C. 102 (e) as being anticipated by Ben-Ze'ev et al, Patent 6,687,787, hereinafter Ben-Ze'ev et al. This rejection is not thought to be well taken.

While it is true that Ben-Ze'ev et al show both a processor and coprocessor constituting each processing unit 253, 254, they are connected to perform different functions from those taught and claimed in the instant application. For example, as claimed in method claim 1 and structure claim 7, the processor takes a data packet, makes it into a frame with headings and then passes the frame with the headings to the coprocessor, which coprocessor performs any operations required by the header, modifies the header and returns the frame to the processor. The processor then transmits the packet with the modified heading on the network. This is not taught nor suggested by Ben-Ze'ev et al. First, the coprocessor may receive data from the bus directly. "The processor 400 and coprocessor 401 each have access to the tubular bus...." In applicants' method and structure, the coprocessor gets the data frame composed by the processor and acts only on the heading. In Ben-Ze'ev et al, the coprocessor acts on the data, e.g. DES and CRL, and not just to modify the heading. In applicants' application, the coprocessor always returns the frame to the processor for transmission on the network. None of this is taught or suggested by Ben-Ze'ev et al. The examiner refers to col. 12, lines13-35, and col. 11, lines 8-44, for some of these features, but these locations refer only to the processing unit(s) and not to the interaction of the coprocessor and processor.

Prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v.

Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984).

"Anticipation requires identity of the claimed process and a process of the prior art; the claimed process, including each step thereof, must have been described or embodied, either expressly or inherently, in a single reference" Glaverbel Societe Anonyme v. Northlake Marketing & Supply, Inc. 45 F. 3d 1550, 1554, 33 USPQ2d 1496, 1498 (Fed. Cir. 1995).

A possibility or probability that features of the prior art contained in the disclosure of the prior art is not enough to establish anticipation. The same characteristics must be a "natural result flowing" from what is disclosed (Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed Cir. 1991). Clearly, Ben Ze'ev et al do not show each step and each structure.

With respect to claims 2-6 and 8-12, these are dependent, directly or indirectly, on claims 1 and 7, respectively, and for the same reasons are believed to be allowable. Moreover, claims 2 and 8 require that all data with created headers be sent to the coprocessor and returned to the processor in the order it was received. This is neither taught nor suggested by Ben-Ze'ev et al, and especially not at the location cited (col. 12, lines 57-67). While the information is delivered from the coprocessor to a FIFO, this speaks only to the information *after* it is delivered from the coprocessor, not the order in which it is delivered *from* the coprocessor. Thus, for this additional reason, claims 2 and 8 are believed to be allowable.

Claims 3 and 9 require that the processor used to transmit data be able to receive data with the modified header, pass this to the coprocessor, which restores the original header, and return the frame to the processor. It is neither taught nor suggested by Ben-Ze'ev et al that a single processor-coprocessor unit can act to send and receive and, for this additional reason, claims 3 and 9 are believed to be allowable.

With respect to claims 4 and 10, these require that there be two processors connected to pass data therebetween. It is submitted that this is not taught nor suggested by Ben-Ze'ev et al, especially at the location cited by the examiner where the processors and coprocessors are handled only as a unit, and not individually. Thus, for this additional, reason claims 4 and 10 are believed to e allowable.

With respect to claims 5, 6, 11 and 12, it is submitted that there is no teaching where any information for creating headers is located, and this is not taught nor suggested by Ben-Ze'ev et al. Thus, for this additional reason, claims 5, 6, 11 and 12 are believed to be allowable.

For the above reasons, each of the claims now in the application is distinguishable, one from the other and over the prior art. Therefore, reconsideration and allowance of each of the claims now in the application is respectfully requested.

Respectfully submitted,

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